WHAT IS CLAIMED IS:

1. A method of manufacturing a thin film transistor, comprising:

preparing a substrate and a mixed solution, the mixed solution having a reductant and a first metal;

forming a photoresist pattern on the substrate;

etching a portion of the substrate to form a groove using the photoresist pattern as a mask;

depositing a second metal on the substrate, a height of the second metal being smaller than a depth of the groove;

removing the photoresist pattern on the substrate and the second metal on the photoresist other than in the groove; and

forming the first metal on the second metal in the groove by submerging the substrate in the mixed solution.

2. The method of claim 1, wherein the first metal is a copper (Cu).

3. The method of claim 2, wherein the mixed solution includes a sulfuric acid (H_2SO_4) and a cupric sulfate ($CuS0_4 \cdot 5H_20$).

4. The method of claim 3, wherein the reductant is one of a formaldehyde (HCHO), a hydrazine, a sodium phosphate (NaH_2PO_2), a sodium borate ($NaBH_4$), and a dimethyl amine borane (DMAB).

5. The method of claim 1, wherein the first metal is a silver (Ag).

6. The method of claim 5, wherein the mixed solution includes a silver nitrate ($AgNO_3$), an ammonium hydroxide (NH_4OH), and a sodium hydroxide (NaOH).

7. The method of claim 6, wherein the reductant is one of a formaldehyde, a hydrazine and a glucose.

8. The method of claim 1, wherein the first metal is a gold (Au).

9. The method of claim 8, wherein the mixed solution includes a gold chloride ($AuCl_2$), a sodium chloride (NaCl), and water (H_2O).

10. The method of claim 9, wherein the reductant is one of a formaldehyde, a glucose, a sodium phosphate (NaH_2PO_2), and a N-N-dimethyl glycine sodium.

11. The method of claim 1, wherein the second metal is one of Pd, Pt, Au, Cu, Mo Cr, Ti, Ni, W and Co.

12. The method of claim 1, further comprising:

forming a first insulating layer over the substrate to cover the first metal;

forming a semiconductor layer on the first insulating layer;

forming source and drain electrodes on the semiconductor layer;

forming a second insulating layer over the whole substrate covering the source and drain electrode, the second insulating layer including a contact hole on a portion of the drain electrode; and

forming a pixel electrode on the second insulating layer, the pixel electrode electrically connecting with the drain electrode through the contact hole.

13. The method of claim 12, wherein the first metal is a gate electrode.